Code No: 155AK

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, March - 2021
COMPUTER ARCHITECTURE
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Clearly bring out the differences between RISC and CISC architectures.
b) How does the operation load register from memory function? Explain with steps. [8+7]

2.a) Why is Associative memory referred to as Content Addressable memory? Explain the importance of Associative memory.
b) Explain the concept of Set Associative mapping in Cache memory. [7+8]

3. What is a segment register? Draw and explain the interfacing of 8086 along with its design and interfacing. [15]

4.a) How is the memory organized in 8086?
b) What is segmentation? How it is performed in 8086? [7+8]

5.a) What is stall? What is/ are the solution/ solutions to overcome stalling?
b) How can loop unrolling be performed? [8+7]

6. How can the branch prediction be performed? Explain with the help of flowchart. [15]

7. Draw and explain the hardware architecture for DSP. [15]

8.a) How is latency measured with respect to SoC?
b) How does a simulator work in an MIPS? [8+7]

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